DW780 UNIBUS Adaptor

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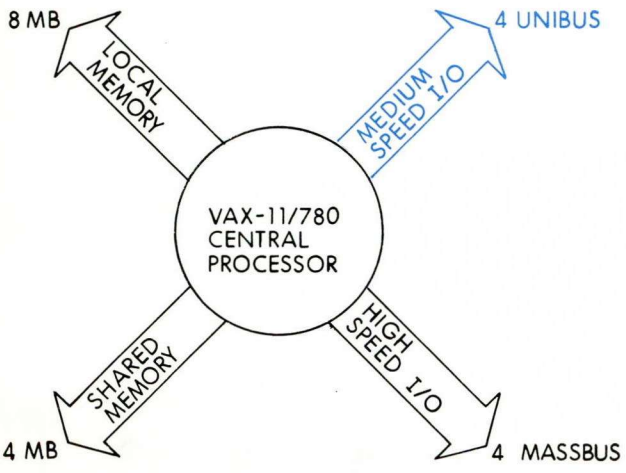
DW780 UNIBUS adaptors provide a unique capability for minicomputers: the ability to support more than one medium-speed I/O channel. VAX-11/780 systems can now support up to four UNIBUS adaptors in addition to four high-performance MASSBUS adaptors. Multiple UNIBUS adaptors increase system throughput by distributing the device load among more than one UNIBUS, thereby making more UNIBUS bandwidth available to each device.



FEATURES

- Direct Memory Access (DMA) data transfers eliminate processor intervention for high data throughput
- Interrupt capability for program I/O devices
- Increases flexibility in peripheral selection
- Provides a means for connecting user-designed devices
- Increases system throughput by distributing the load of several UNIBUS devices among up to four UNIBUS adaptors

DESCRIPTION

The VAX-11/780 UNIBUS connects most peripheral devices to the VAX-11/780 processor. The UNIBUS, which is an asynchronous bidirectional interconnect, offers the largest selection of peripheral devices of any of DIGITAL's system interconnects. These devices include medium-capacity disks, unit record devices, terminals, interprocessor communications links, and user-designed peripherals, plus all DIGITAL- and user-developed real-time devices. The UNIBUS on the VAX-11/780 is the same as the PDP-11 UNIBUS. Thus existing UNIBUS peripheral device interfaces can be used without modification on VAX-11/780 systems. However, I/O drivers and diagnostics that are compatible with VAX/VMS and the VAX I/O architecture must be provided.

Device-related addresses, data, and control information are passed along the 56 lines of the UNIBUS. The DW780 UNIBUS adaptor (UBA) provides the hardware pathways and protocol for this information to move between the UNIBUS and the processor's Synchronous Backplane Interconnect (SBI) and performs priority arbitration among UNIBUS devices. The maximum aggregate throughput rate of the VAX-11/780 UNIBUS is 1.39 million bytes per second.

DW780 Operation

Processor Access of UNIBUS Device Registers— The UNIBUS address space for each of the four UNIBUSes is included within the SBI address space. Each DW780 translates an SBI access into a UNIBUS access, which corresponds to its UNIBUS address space, thereby allowing the processor to read or write a UNIBUS device's registers.

Direct Memory Access— The DW780 translates UNIBUS device Direct Memory Access (DMA) transfers to SBI memory accesses. The DW780 address translation map translates an 18-bit UNIBUS address to a 30-bit SBI address. The map provides direct access to system memory for DMA UNIBUS peripheral devices and permits scatter/gather transfers on a page by page basis.

To make the most efficient use of the SBI bandwidth, the DW780 provides Buffered Data Paths for up to 15 device transfers. Each of these channels has a 64-bit buffer (plus byte-parity) for holding four 16-bit words for DMA transfers between a UNIBUS device and memory. The result is that only one SBI transfer (64 bits) is required for every four UNIBUS transfers. The maximum aggregate transfer rate through the buffered data paths is 1.39 million bytes per second. On memory read transfers, the DW780 anticipates upcoming UNIBUS requests by pre-fetching the next 64-bits from memory as the last 16-bit word is transferred from the buffer to the UNIBUS. By the time the UNIBUS device requests the next word, the DW780 has it ready to transfer.

Any number of unbuffered DMA transfers are handled by one Direct Data Path. Every 8- or 16-bit transfer requires one 32-bit transfer on the SBI. The maximum transfer rate through the Direct Data Path is 850K bytes per second for writes to memory and 635K bytes per second for memory read accesses.

Program I/O Transfers—The DW780 provides for program I/O transfers by maintaining an interrupt structure between a UNIBUS device and the processor. Once the processor is interrupted and vectored into an interrupt service routine it can then access the UNIBUS device's registers to service the interrupt.

The DW780 permits concurrent program interrupt, unbuffered, and buffered data transfers. The aggregate throughput rate when using the Direct Data Paths and any of the 15 buffered data paths is between 635K bytes per second and 1.39M bytes per second.

Multiple DW780s

Where system applications require greater I/O throughput than one UNIBUS can handle, the VAX-11/780 supports up to four UNIBUS adaptors. When assigning devices to multiple UNIBUSes, one of the main concerns is DMA transfer latency tolerance. Latency is defined as the length of time required to perform a DMA transfer, and is a function of device throughput, device silo characteristics, and device transfer cycle overhead.

The devices that are the least latency tolerant should be assigned to the highest priority UBA. Generally, high throughput devices are the least tolerant of increased latency.

Configuration Requirements

Any device can be attached to any UNIBUS as long as the normal UNIBUS loading and sequencing configuration rules are followed. One exception is any system that uses the RK07 as a system device. If the system has multiple UNIBUSes and one RK711 controller, the RK711 must be placed on the highest priority DW780. If multiple RK711 controllers are attached to multiple DW780s, and any one could be used as a system device, then they must be attached to consecutive DW780s in descending priority order. This is a restriction imposed by the system bootstrap program.

The DW780 is a self-contained, 4-inch backplane with power supply—the same size as a MASSBUS adaptor. In RK07-based packaged systems, a DW780 can be mounted either in the central processor cabinet or in a CPU expander cabinet (H9602-HA/HB); in RM03- and RP06-based packaged systems, a DW780 can be mounted in a CPU expander cab.

SOFTWARE SUPPORT

The VAX-11/780 operating system, VAX/VMS, and its diagnostic system support up to four DW780 UBAs. Programmers need not be concerned to which DW780 a particular device is attached since total program transparency has been maintained.

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